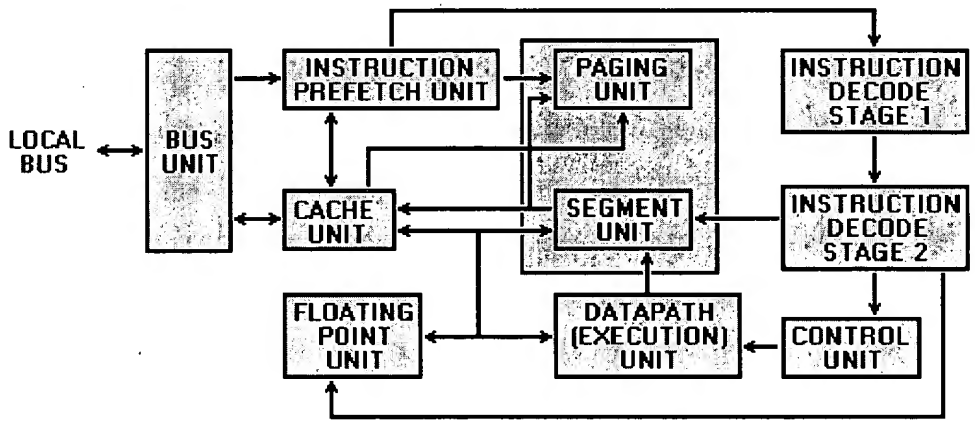
486 FUNCTIONAL DESCRIPTION

The 486 processor family enables a range of low- cost, high- performance entry- level system designs capable of running the entrie installed base of DOS, MS- Windows, OS/2, UNIX, and RTOS applications written for the Intel architecture. The 486 processor family offers the full binary compatibility with 8086, 8088, 80286, and 80386 EX/SX/DX processors. All of the 486 processors integrates an 8- Kbyte or 16- Kbyte unified internal cache for both data and instructions. Cache hits provides zero waitstate access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain the cache consistency. All of the 486 processor family members also contains a 32- bit RISC integer processing unit for 8-, 16-, and 32- bit data types using a full- width ALU and eight 32- bit general purpose registers. The 486 processors also offers a memory management unit.



486 Bus Unit: The bus unit provides the physical interface between the 486 processor and the external devices. The bus unit consists of the address drivers and receivers, write buffers, data bus transceivers, bus size control logic, bus control request sequencer, burst bus control logic, cache control logic, and the parity generation and checking logic.

- **Address drivers/receivers:** When the 486 processor is executing a bus cycle, the address drivers are used to drive the address out onto the processor's local address bus (A31:A2) and the byte enable lines. During cache invalidation cycles, address bits A31:A4 are input from the processor's local address bus through the address receivers.
- **Write buffers:** The four write buffers of an 486 processor allow the bus unit to buffer up to four write bus cycles from the processor, permitting these write operations to complete execution instantly.
- **Data bus receivers:** The 486 data bus receivers are used to gate data onto the processor's local data bus during 486 write bus cycles. The data bus receivers are also used to gate data into the processor from the processor's local data bus during 486 read bus cycles.
- **Bus size control logic:** The bus size control logic is used, when the processor is communicating with 8- or 16- bit devices. If necessary, the processor automatically executes multiple bus cycles for 8- and 16- bit devices.
- **Bus control request sequencer:** The bus control request sequencer determines the order of addressing during burst transfers.
- **Burst bus control logic:** The burst bus control logic is used to control the buses during the execution of burst transfers.

- **Cache control logic:** The cache control logic connects the 486 processor local buses to an

external cache controller.

- **Parity generation and checking logic:** This logic automatically generates even parity on data being written by the 486 processor and checks for valid even parity during 486 read bus cycles.

486 Cache Unit: The 486 processor family members contains an internal cache controller and an 8- Kbyte or 16- Kbyte on- chip cache. The on- chip cache is a unified code and data cache. The cache is used for both data and instruction accesses and acts on physical addresses. The cache organisation is 4- way set associative and each line is 16 bytes wide. The cache memory are logically organized as 128 sets, each containing four lines. The on- chip cache is software transparent to maintain binary compatibility with previous generations of the Intel 80x86 architecture.

Floating Point Unit: The 486 floating point unit (FPU) executes the same instruction set as the 80387 Numeric Coprocessor extension. It shares microcode ROM, instruction decode and address pipeline logic with the datapath, or integer execution unit. The FPU provides arithmetic instructions for a variety of numeric data types and executes numerous build-in transcendental functions (e. g., tangent, sine, cosine, and log). The FPU fully conforms to the ANSI / IEEE standard 754- 1985 for floating point arithmetic.

Memory Management Unit: The memory management unit (MMU) translates the linear address supplied by the integer processing unit into a physical address to be used by the cache unit and the bus unit. 486 memory management procedures are x86- compatible, adhering to standard paging mechanismus. The 486 MMU consists of two sub- units:

- **The segmentation unit:** The segmentation unit calculates effective (paging unit off) and linear (paging unit on) addresses from the segment and offset. It has been redesigned to generate one address per clock. The segmentation unit contains the segment descriptor cache. It also performs limit and access rights checks.
- **The paging unit:** The paging unit translates the linear address to a physical address. It performs the same functions as the 80386 processor paging mechanism, but has been optimized to improve system performance. It can perform one translation look- aside buffer (TLB) lookup per clock. Individual pages may now be write- protected against supervisor access.
